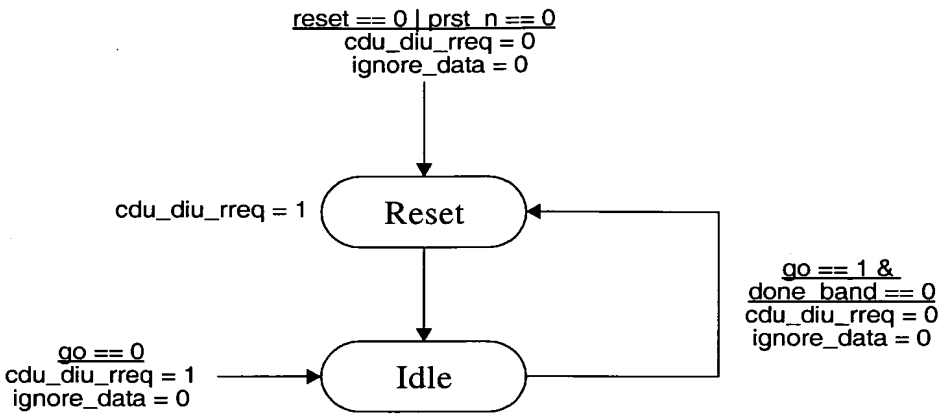

FIG. 1

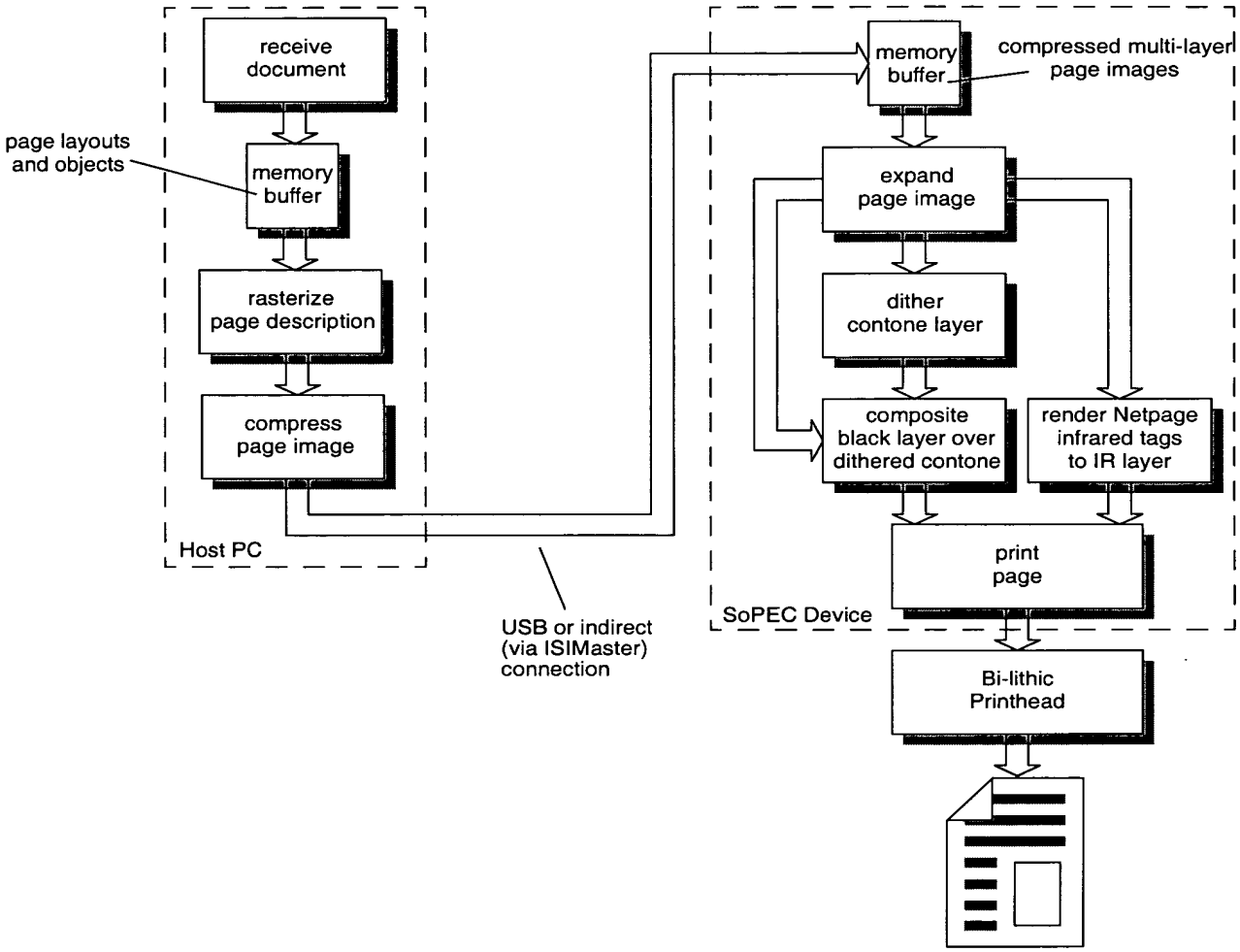
receive document
page layouts and objects
memory buffer
rasterize page description
compress page image
Host PC
USB or indirect (via ISIMaster) connection
memory buffer
compressed multi-layer page images
expand page image
dither contone layer
composite black layer over dithered contone
render Netpage infrared tags to IR layer
print page
SoPEC Device
Bi-lithic Printhead

FIG. 2

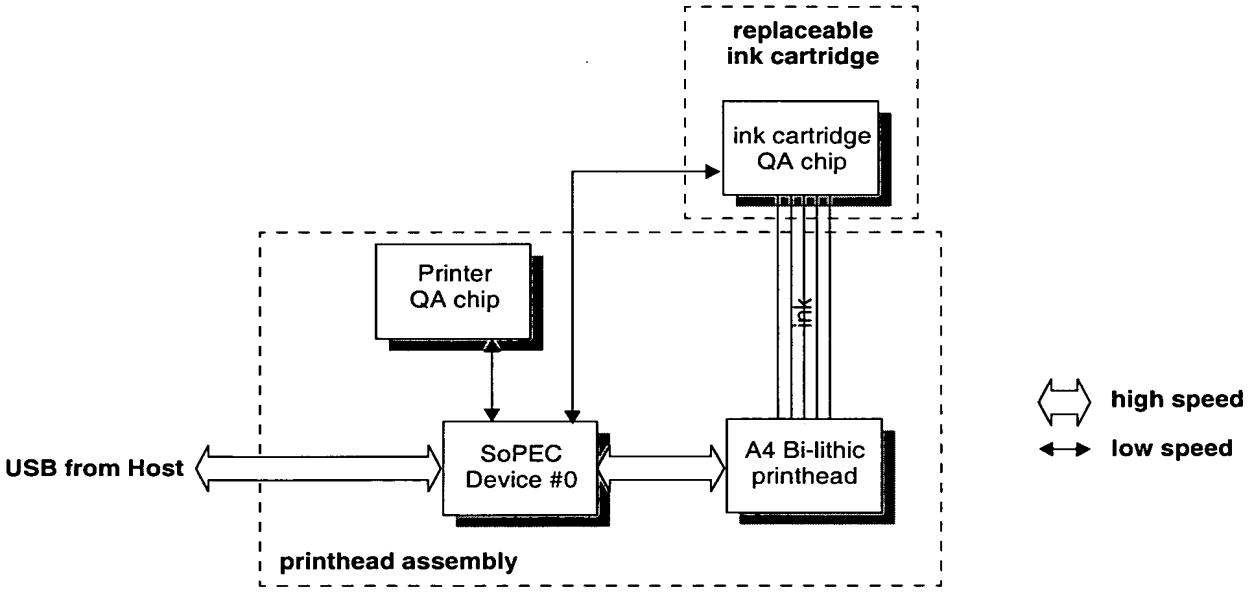
replaceable
ink cartridge
ink cartridge
QA chip
Printer
QA chip
SoPEC
Device #0
A4 Bi-lithic
printhead
USB from Host
printhead assembly
high speed
low speed

FIG. 3

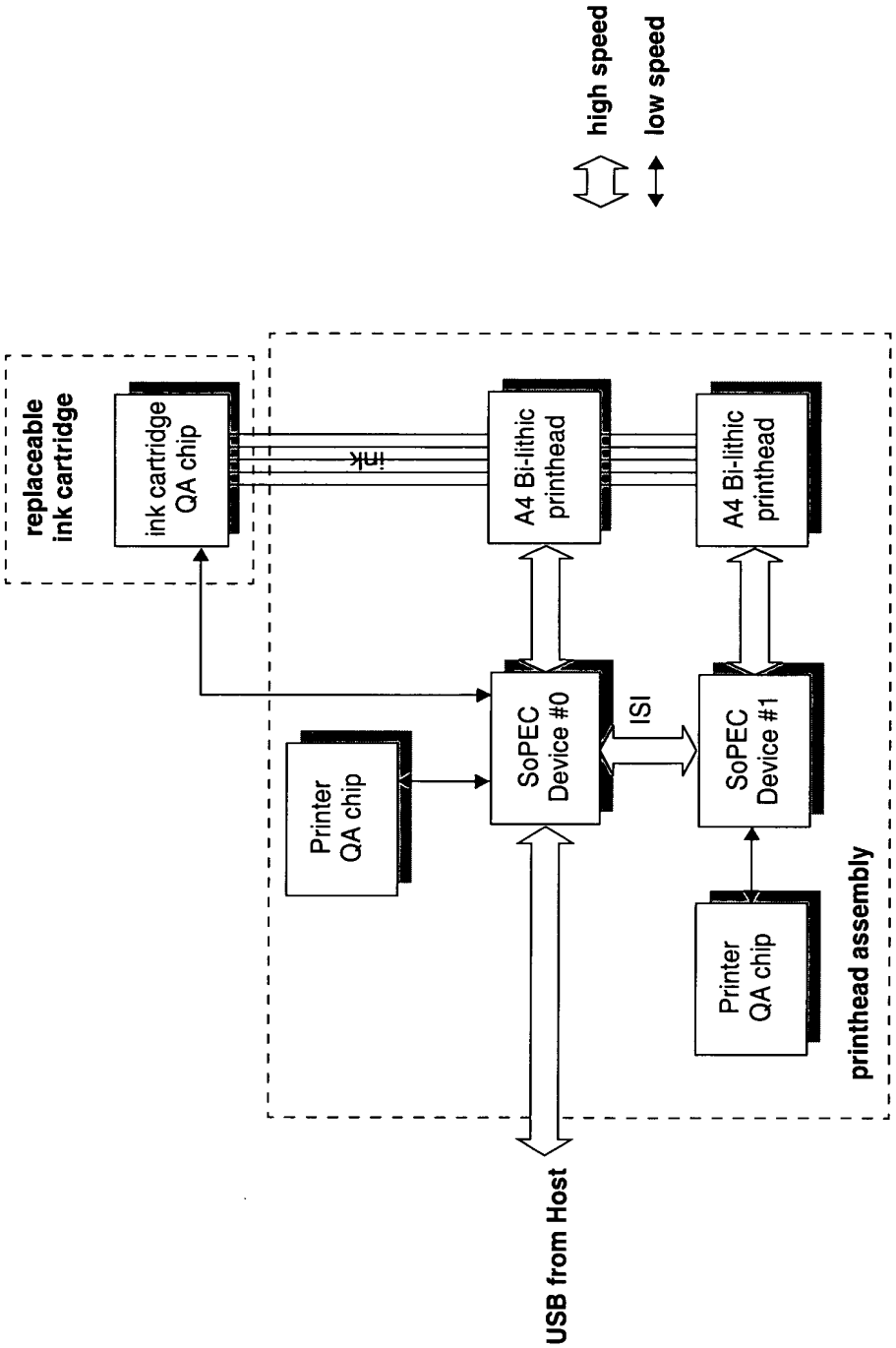
high speed
low speed
replaceable ink cartridge
ink cartridge QA chip
nk
A4 Bi-lithic printhead
A4 Bi-lithic printhead
SoPEC Device #0
ISI
SoPEC Device #1
Printer QA chip
Printer QA chip
printhead assembly
USB from Host

FIG. 4

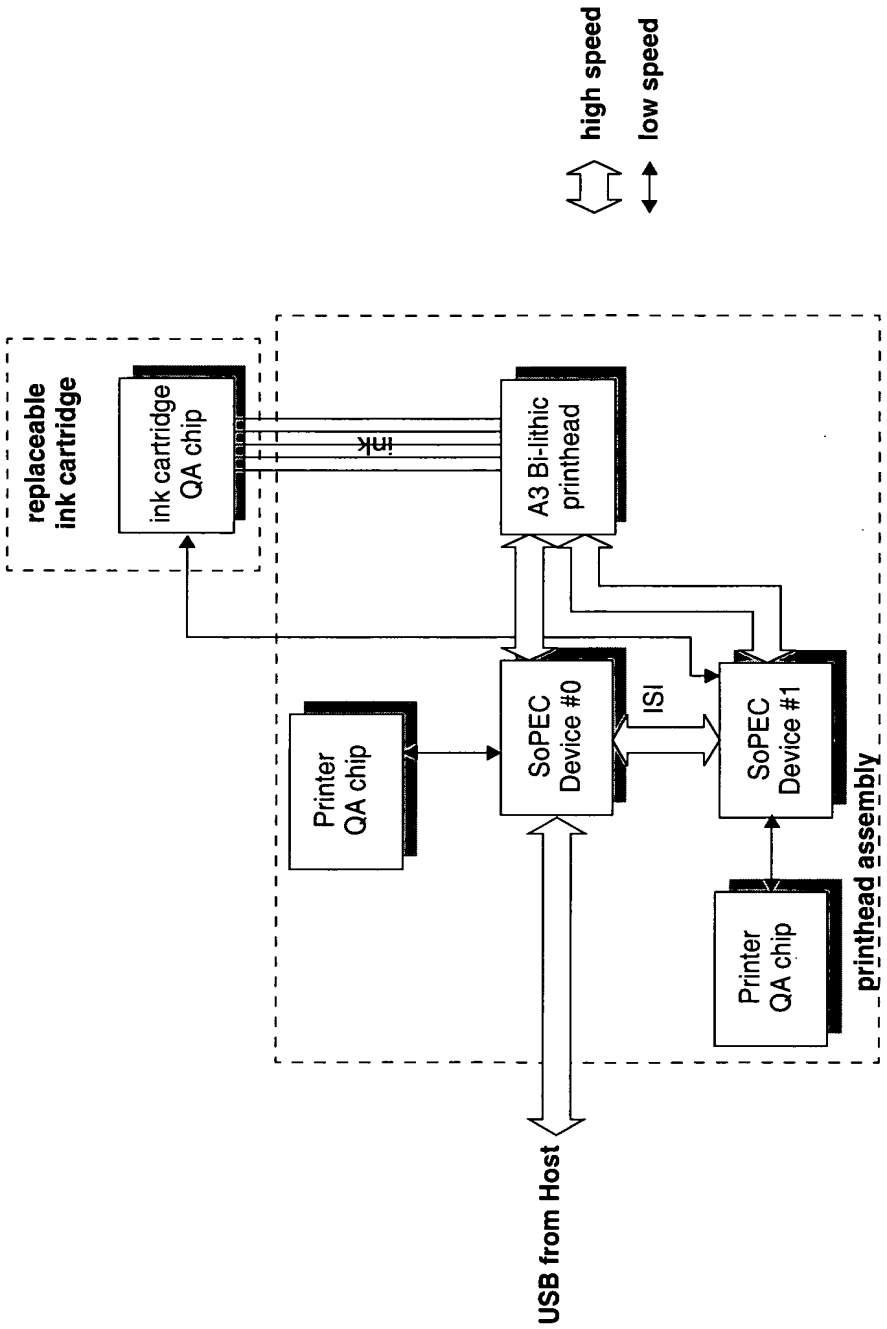
high speed
low speed
replaceable ink cartridge
ink cartridge QA chip
ink
A3 Bi-lithic printhead
SoPEC Device #0
ISI
SoPEC Device #1
Printer QA chip
Printer QA chip
printhead assembly
USB from Host

FIG. 5

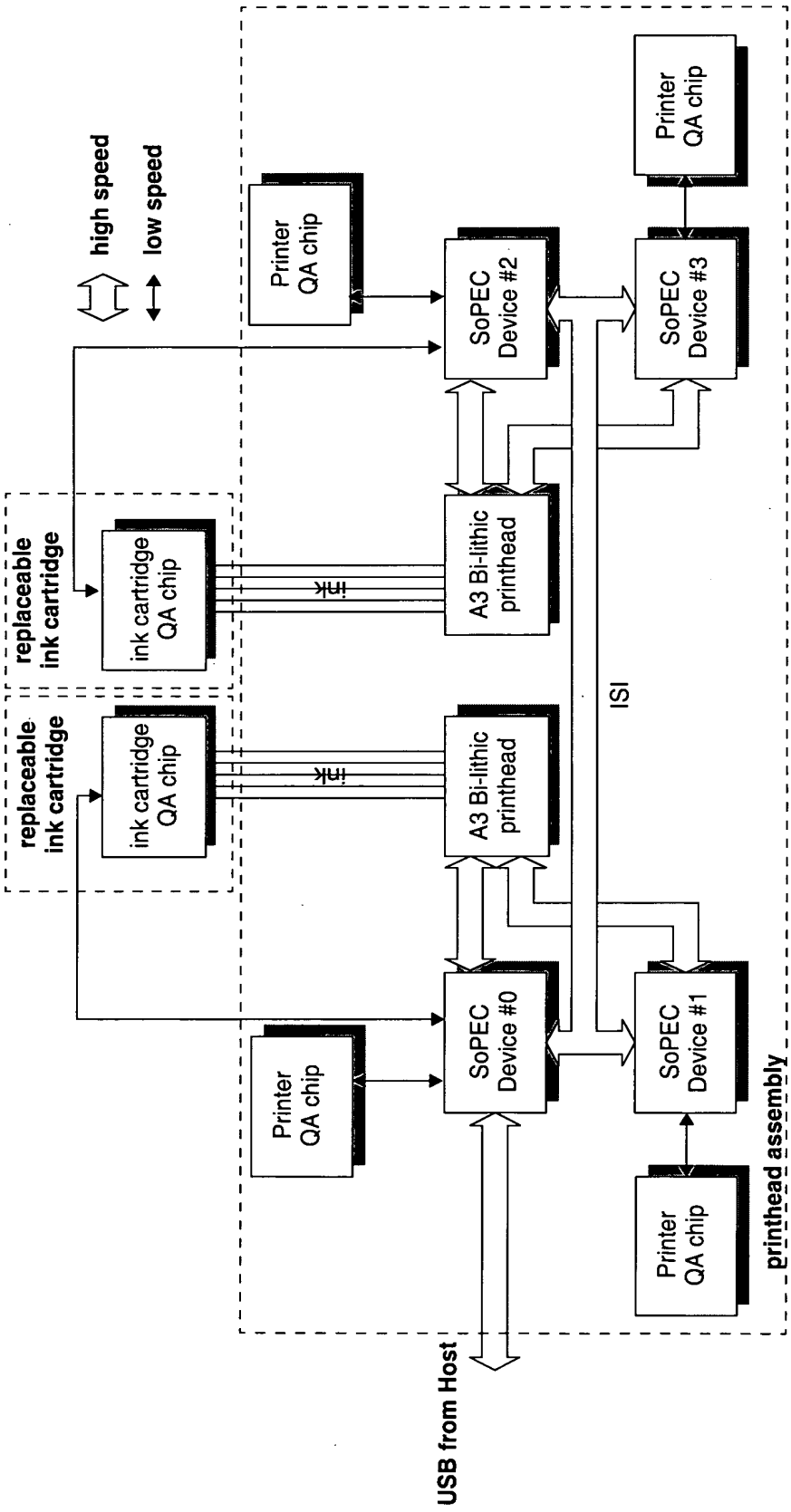
high speed
low speed
Printer QA chip
SoPEC Device #2
Printer QA chip
SoPEC Device #3
replaceable ink cartridge
ink cartridge QA chip
ink
A3 Bi-lithic printhead
ISI
replaceable ink cartridge
ink cartridge QA chip
ink
A3 Bi-lithic printhead
Printer QA chip
SoPEC Device #0
SoPEC Device #1
Printer QA chip
printhead assembly
USB from Host

FIG. 6

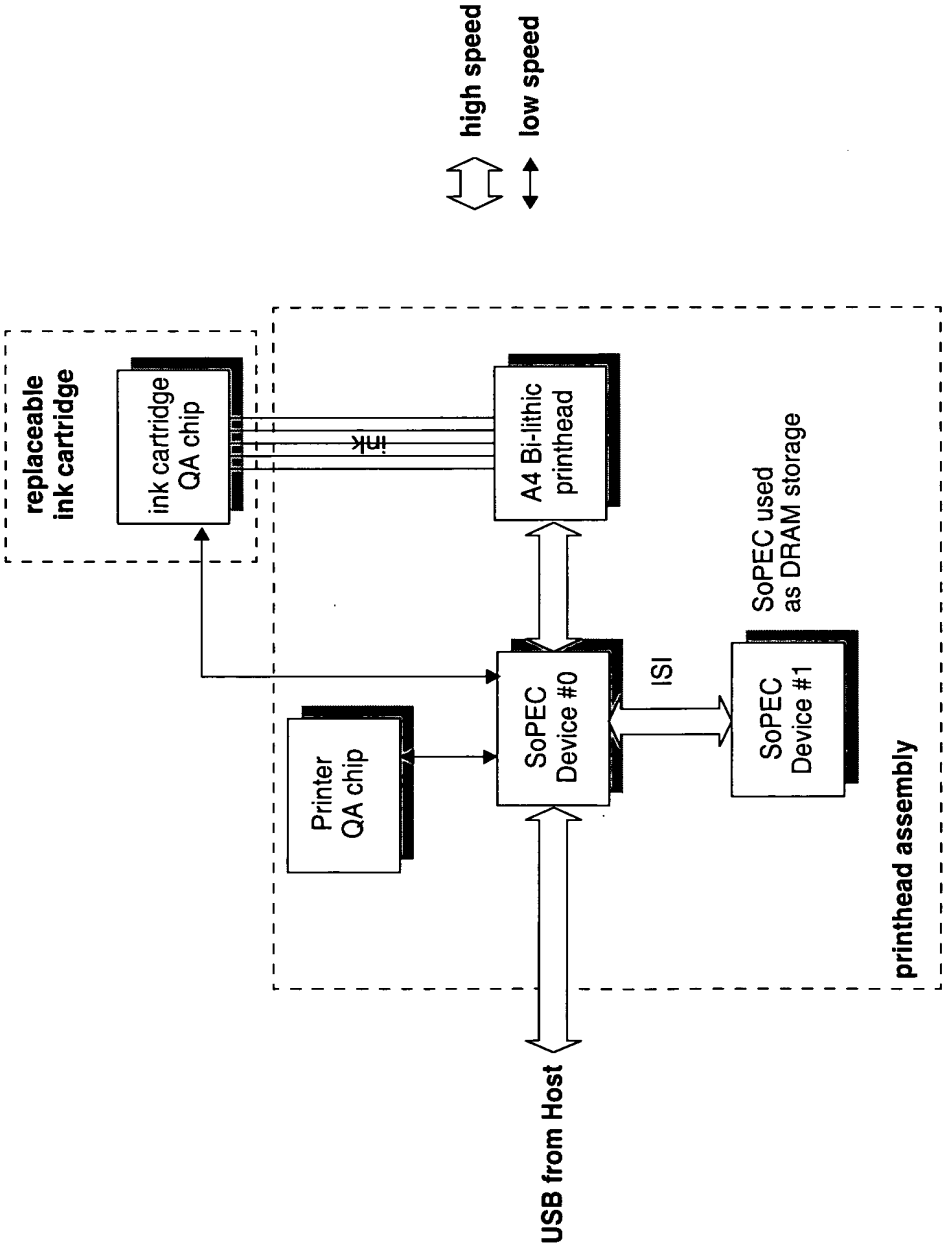
high speed
low speed
replaceable ink cartridge
ink cartridge QA chip
A4 Bi-lithic printhead
SoPEC used as DRAM storage
Printer QA chip
SoPEC Device #0
ISI
SoPEC Device #1
printhead assembly
USB from Host

FIG. 7

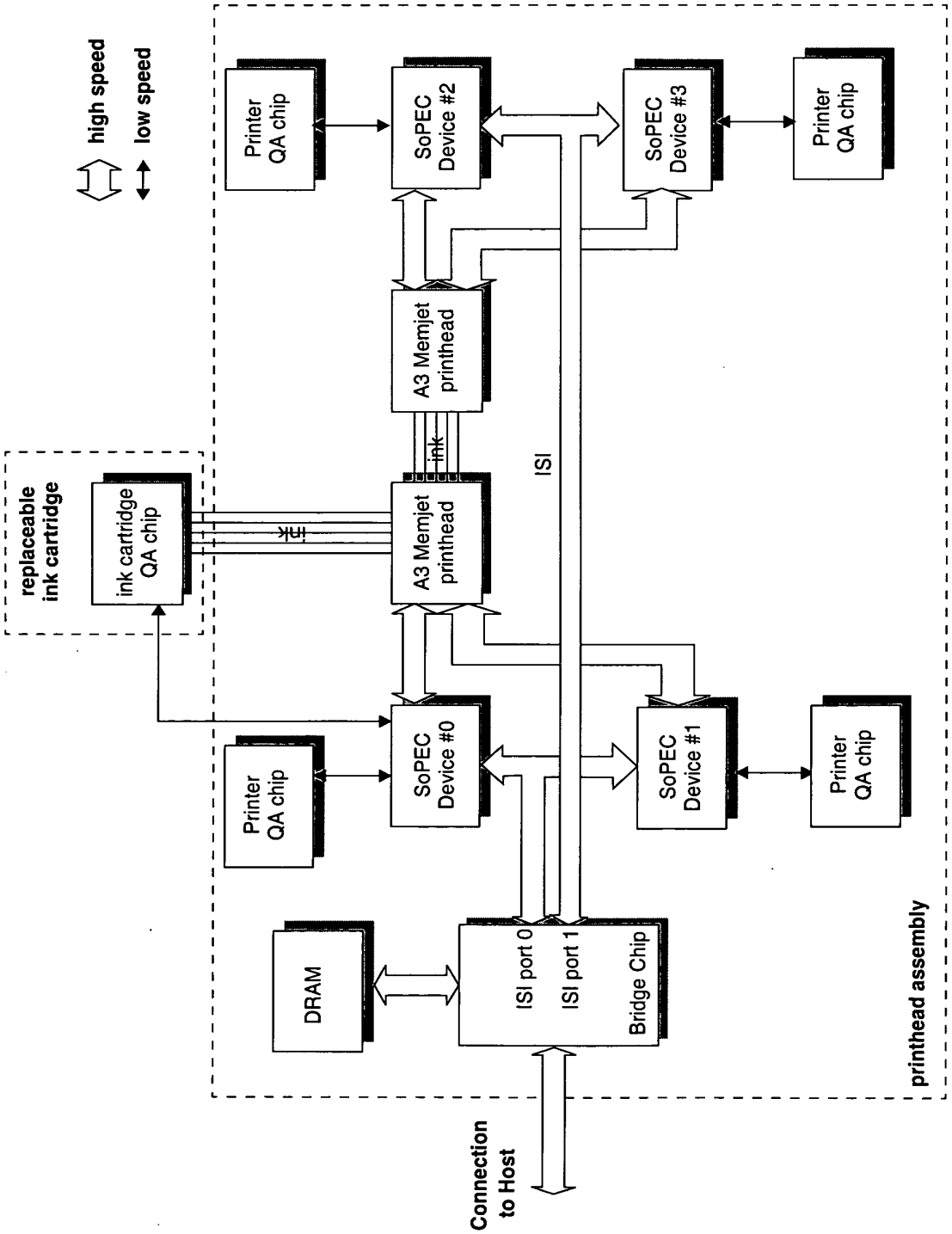
high speed
low speed
Printer QA chip
SoPEC Device #2
SoPEC Device #3
Printer QA chip
A3 Memjet printhead
ink
ISI
replaceable ink cartridge
ink cartridge QA chip
A3 Memjet printhead
Printer QA chip
SoPEC Device #0
SoPEC Device #1
Printer QA chip
DRAM
ISI port 0
ISI port 1
Bridge Chip
printhead assembly
Connection to Host

FIG. 8

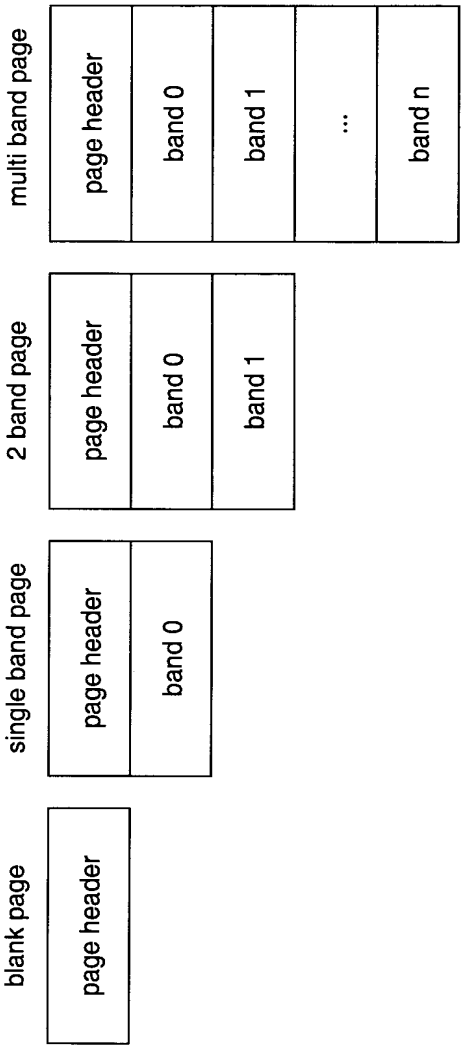
blank page
page header
single band page
page header
band 0
2 band page
page header
band 0
band 1
multi band page
page header
band 0
band 1
...
band n

FIG. 9

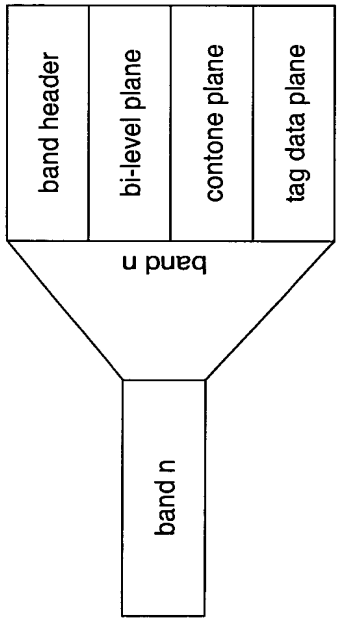
band header
bi-level plane
contone plane
tag data plane
band n
band n

FIG. 10

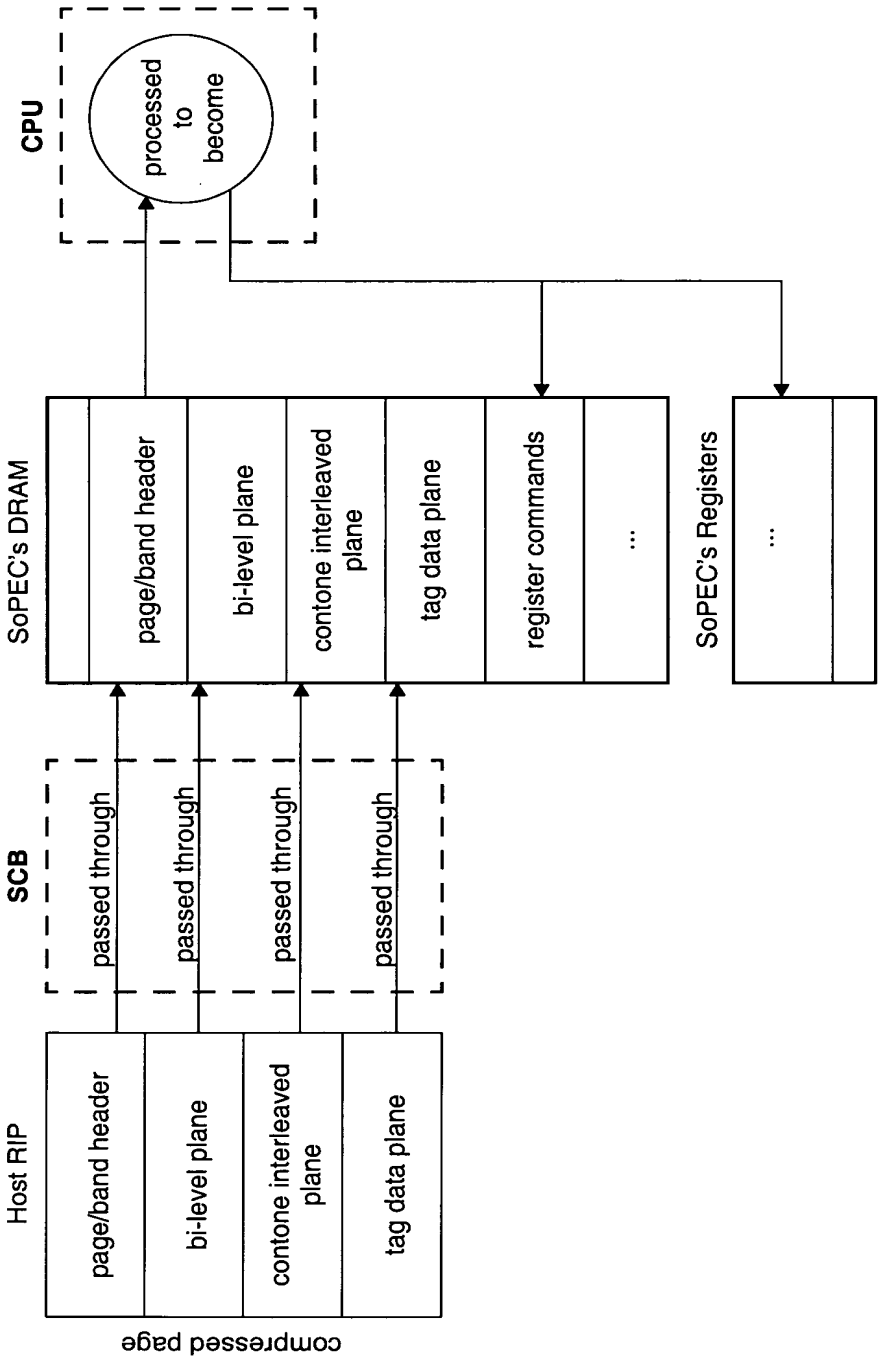
CPU
processed to become
SoPEC's DRAM
page/band header
bi-level plane
contone interleaved plane
tag data plane
register commands
...
SoPEC's Registers
...
SCB
passed through
passed through
passed through
passed through
Host RIP
page/band header
bi-level plane
contone interleaved plane
tag data plane
compressed page

FIG. 11

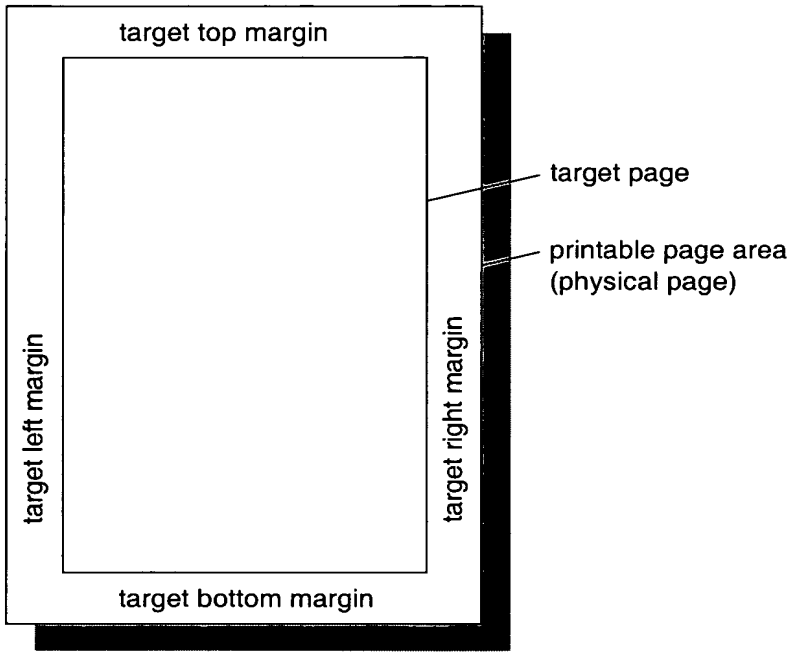
target top margin
target page
printable page area
(physical page)
target left margin
target right margin
target bottom margin

FIG. 12

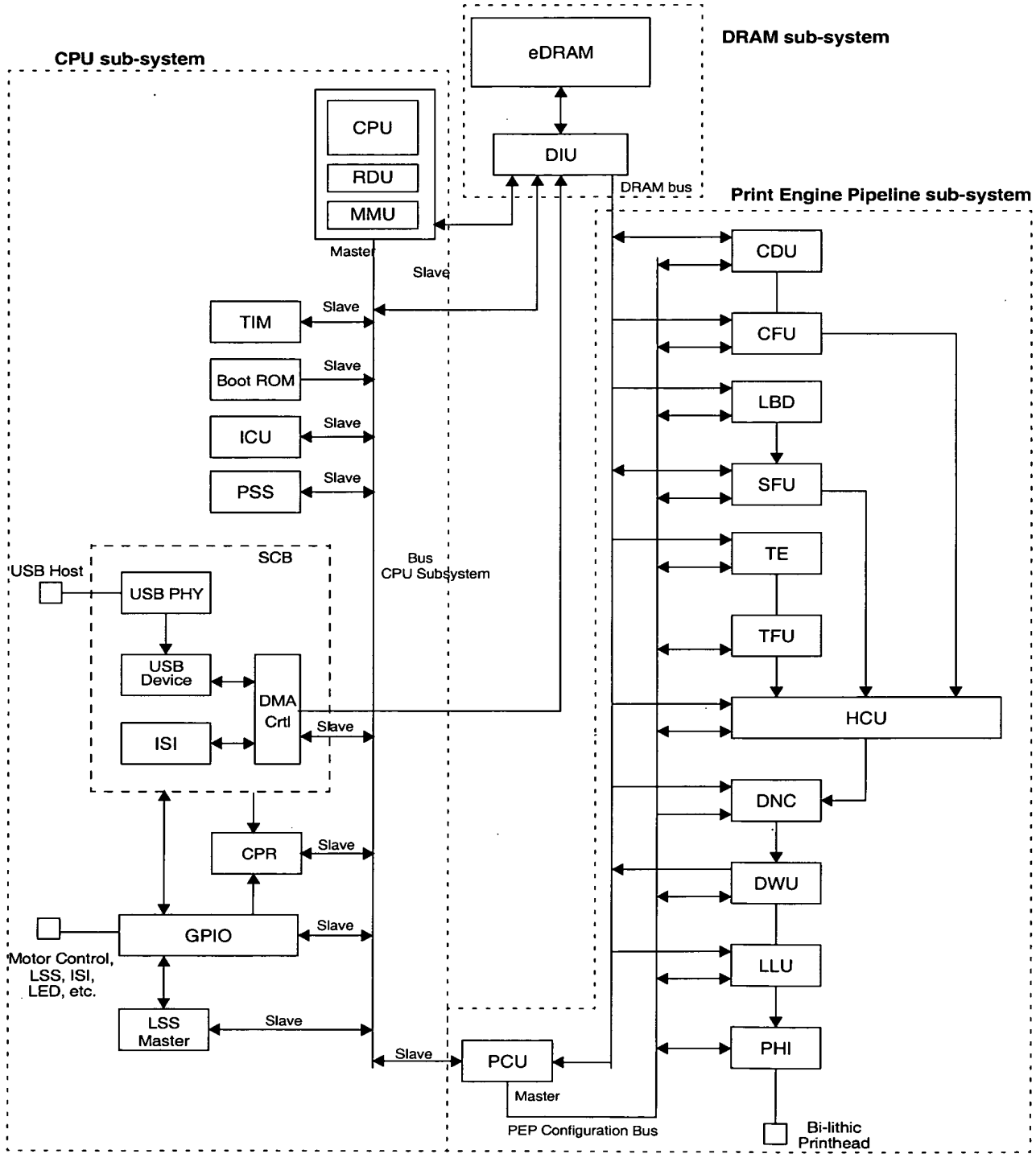
CPU sub-system
DRAM sub-system
eDRAM
DIU
DRAM bus
Print Engine Pipeline sub-system
CPU
RDU
MMU
Master
Slave
TIM
Boot ROM
ICU
PSS
SCB
USB Host
USB PHY
USB Device
ISI
DMA Crtl
Bus CPU Subsystem
CPR
GPIO
Motor Control, LSS, ISI, LED, etc.
LSS Master
PCU
PEP Configuration Bus
CDU
CFU
LBD
SFU
TE
TFU
HCU
DNC
DWU
LLU
PHI
Bi-lithic Printhead

FIG. 13

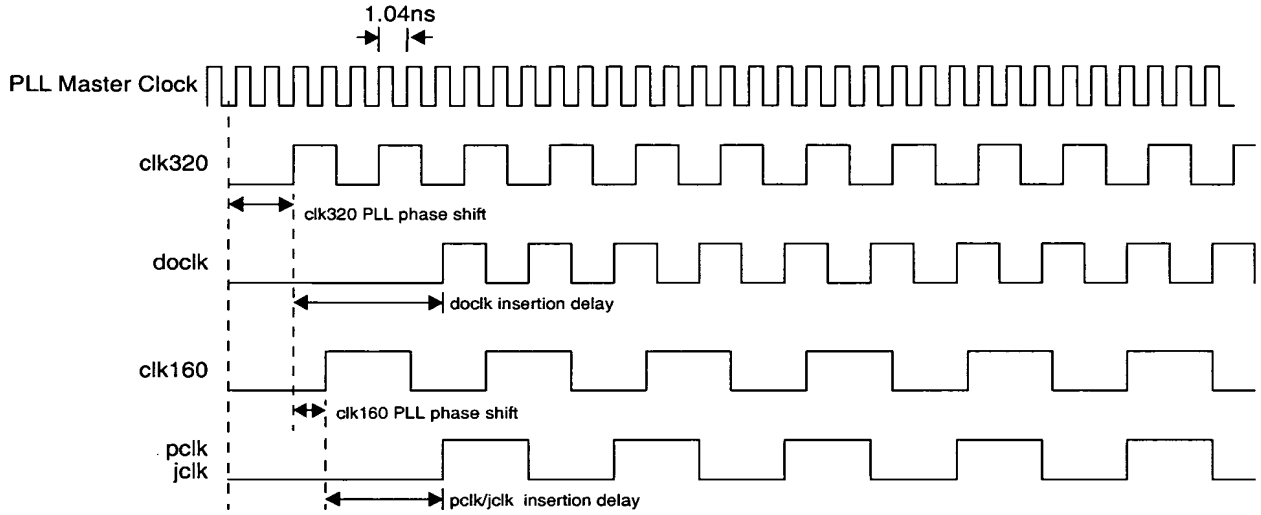
1.04ns
PLL Master Clock
clk320
clk320 PLL phase shift
doclk
doclk insertion delay
clk160
clk160 PLL phase shift
pclk
jclk
pclk/jclk insertion delay

FIG. 14

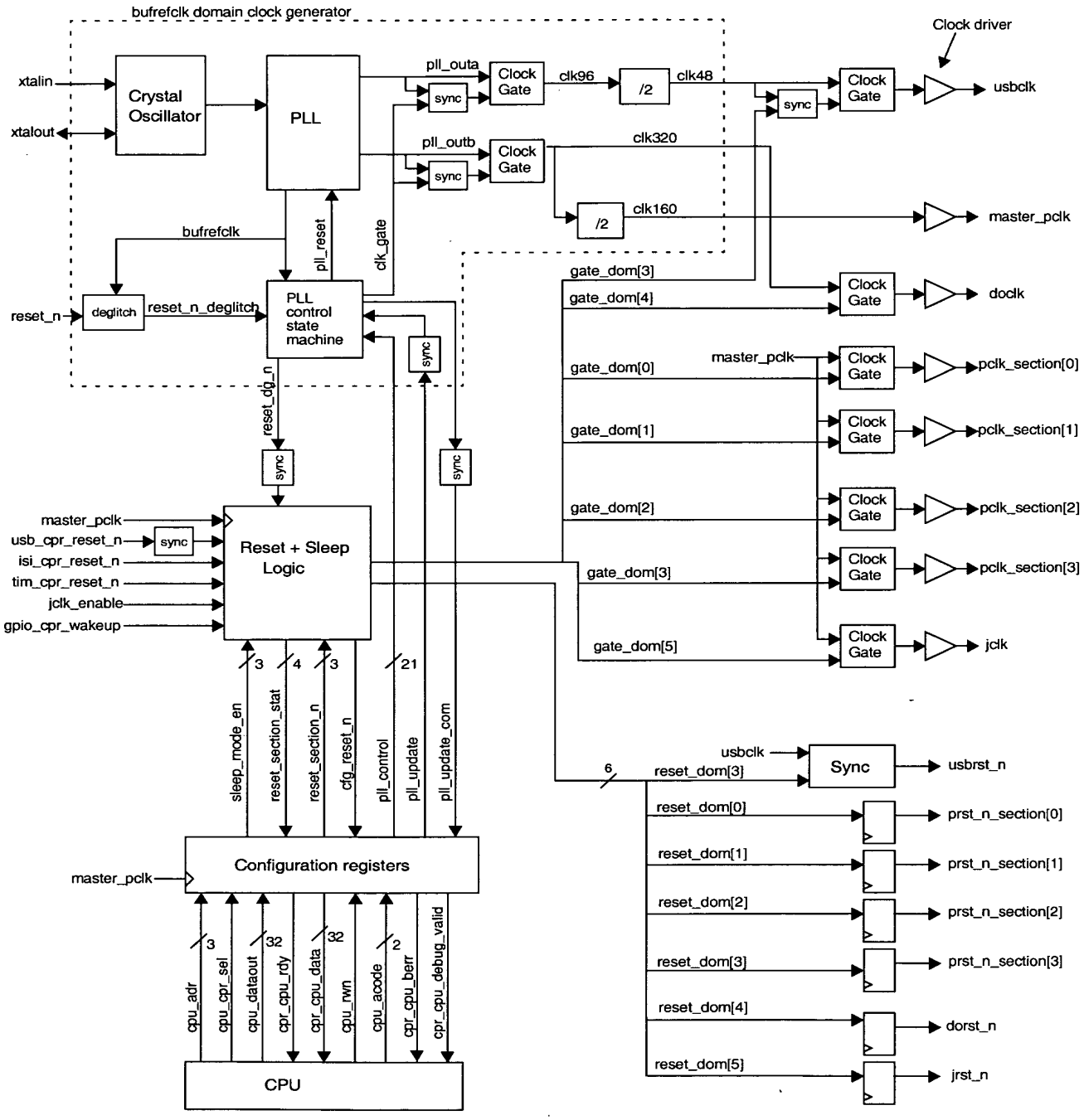
bufrefclk domain clock generator
Clock driver
xtalin
xtalout
Crystal Oscillator
PLL
pll_outa
pll_outb
sync
Clock Gate
clk96
/2
clk48
clk320
clk160
usbclk
master_pclk
doclk
pclk_section[0]
pclk_section[1]
pclk_section[2]
pclk_section[3]
jclk
bufrefclk
pll_reset
clk_gate
reset_n
deglitch
reset_n_deglitch
PLL control state machine
reset_dg_n
gate_dom[3]
gate_dom[4]
gate_dom[0]
gate_dom[1]
gate_dom[2]
gate_dom[5]
usb_cpr_reset_n
isi_cpr_reset_n
tim_cpr_reset_n
jclk_enable
gpio_cpr_wakeup
Reset + Sleep Logic
sleep_mode_en
reset_section_stat
reset_section_n
cfg_reset_n
pll_control
pll_update
pll_update_com
Configuration registers
CPU
cpu_adr
cpu_cpr_sel
cpu_dataout
cpr_cpu_rdy
cpr_cpu_data
cpu_rwn
cpu_acode
cpr_cpu_berr
cpr_cpu_debug_valid
Sync
usbrst_n
reset_dom[3]
reset_dom[0]
reset_dom[1]
reset_dom[2]
reset_dom[4]
reset_dom[5]
prst_n_section[0]
prst_n_section[1]
prst_n_section[2]
prst_n_section[3]
dorst_n
jrst_n

FIG. 15

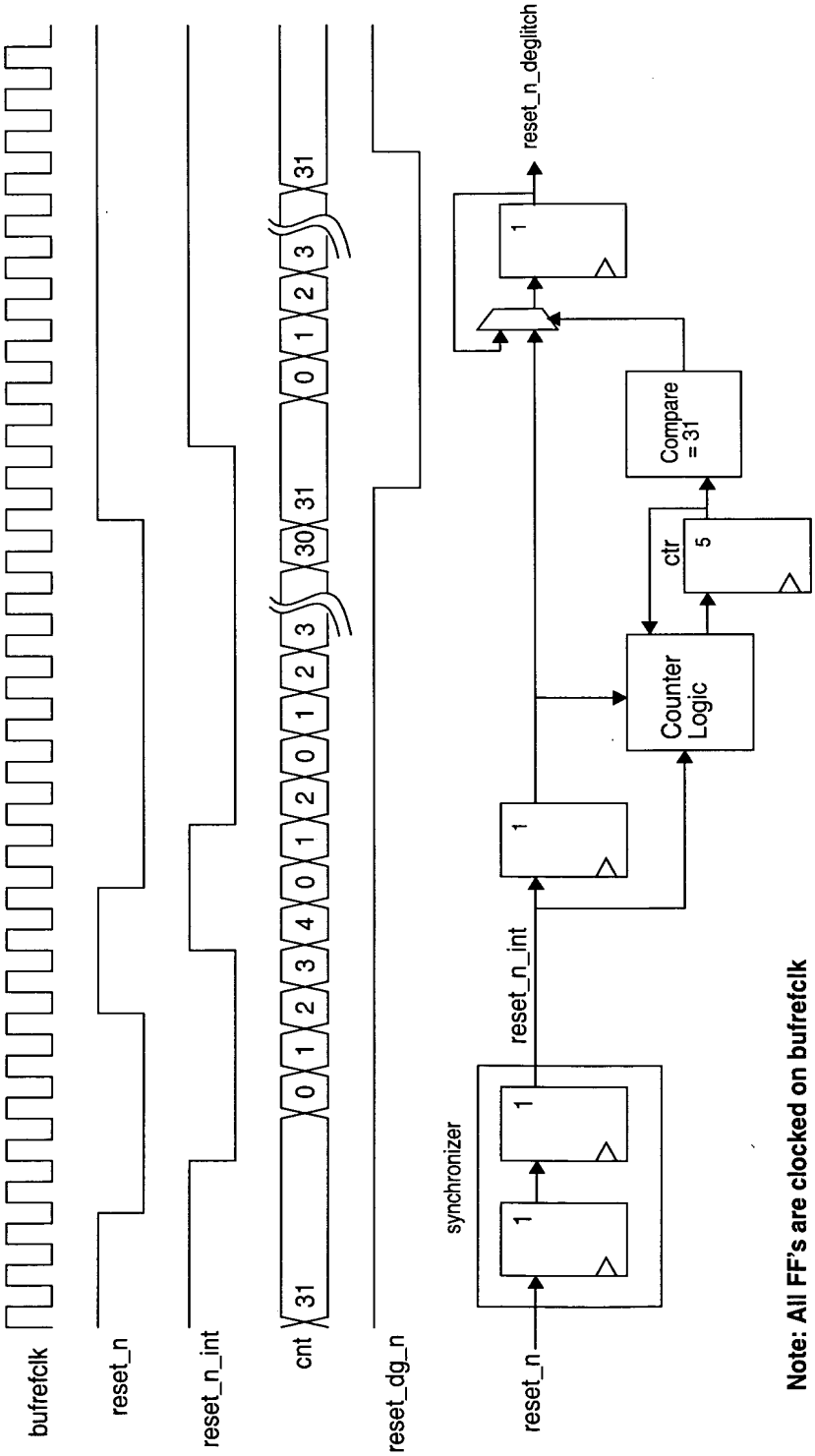
bufrefclk
reset_n
reset_n_int
cnt
reset_dg_n
reset_n
synchronizer
reset_n_int
Counter Logic
ctr
Compare = 31
reset_n_deglitch
Note: All FF's are clocked on bufrefclk

FIG. 16

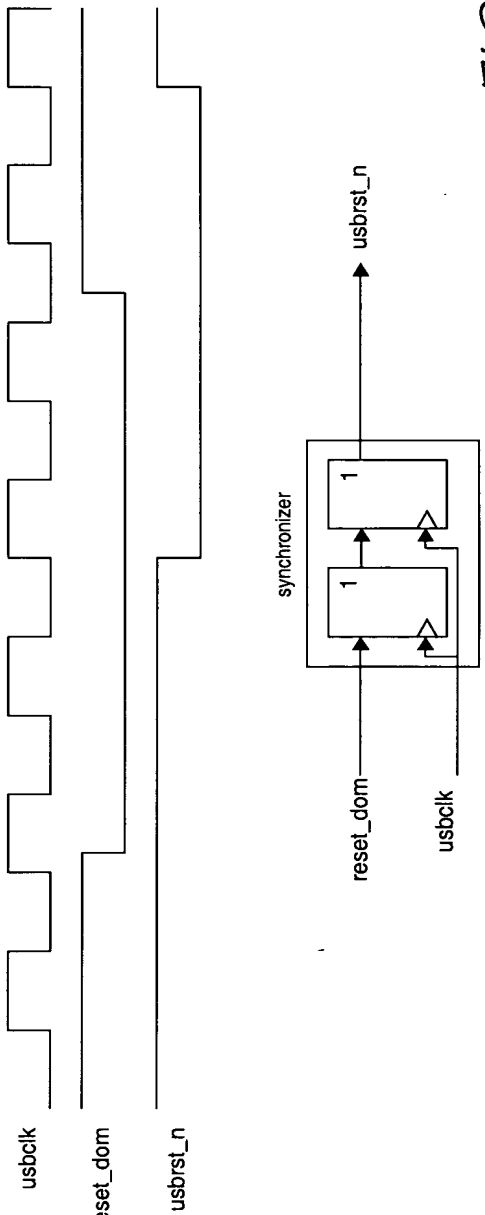
usbclk
reset_dom
usbrst_n
synchronizer
1
1
usbrst_n
reset_dom
usbclk

FIG. 17

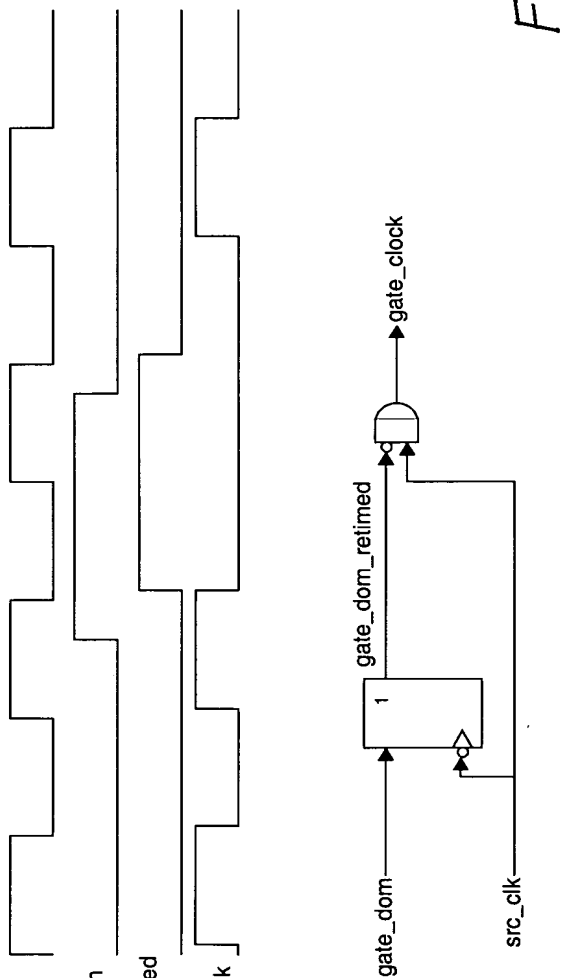
src_clk
gate_dom
gate_dom_retimed
gate_clock
gate_dom_retimed
1
gate_clock
gate_dom
src_clk

FIG. 18

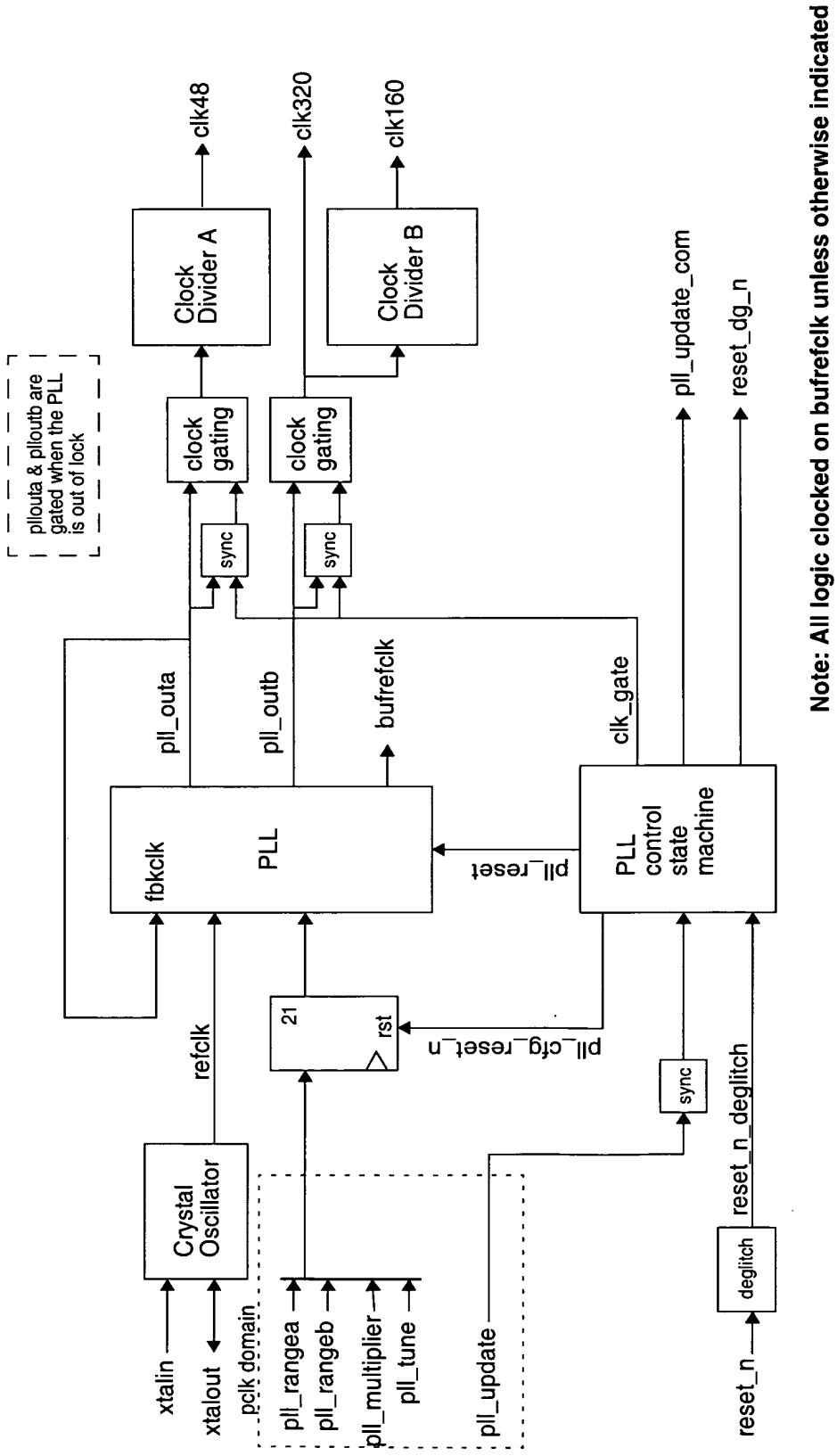
clk48
clk320
clk160
Clock Divider A
Clock Divider B
pllouta & plloutb are gated when the PLL is out of lock
clock gating
clock gating
sync
sync
pll_outa
pll_outb
bufrefclk
clk_gate
pll_update_com
reset_dg_n
fbkclk
PLL
pll_reset
PLL control state machine
Note: All logic clocked on bufrefclk unless otherwise indicated
refclk
21
rst
pll_cfg_reset_n
sync
Crystal Oscillator
reset_n_deglitch
deglitch
xtalin
xtalout
pclk domain
pll_rangea
pll_rangeb
pll_multiplier
pll_tune
pll_update
reset_n

FIG. 19

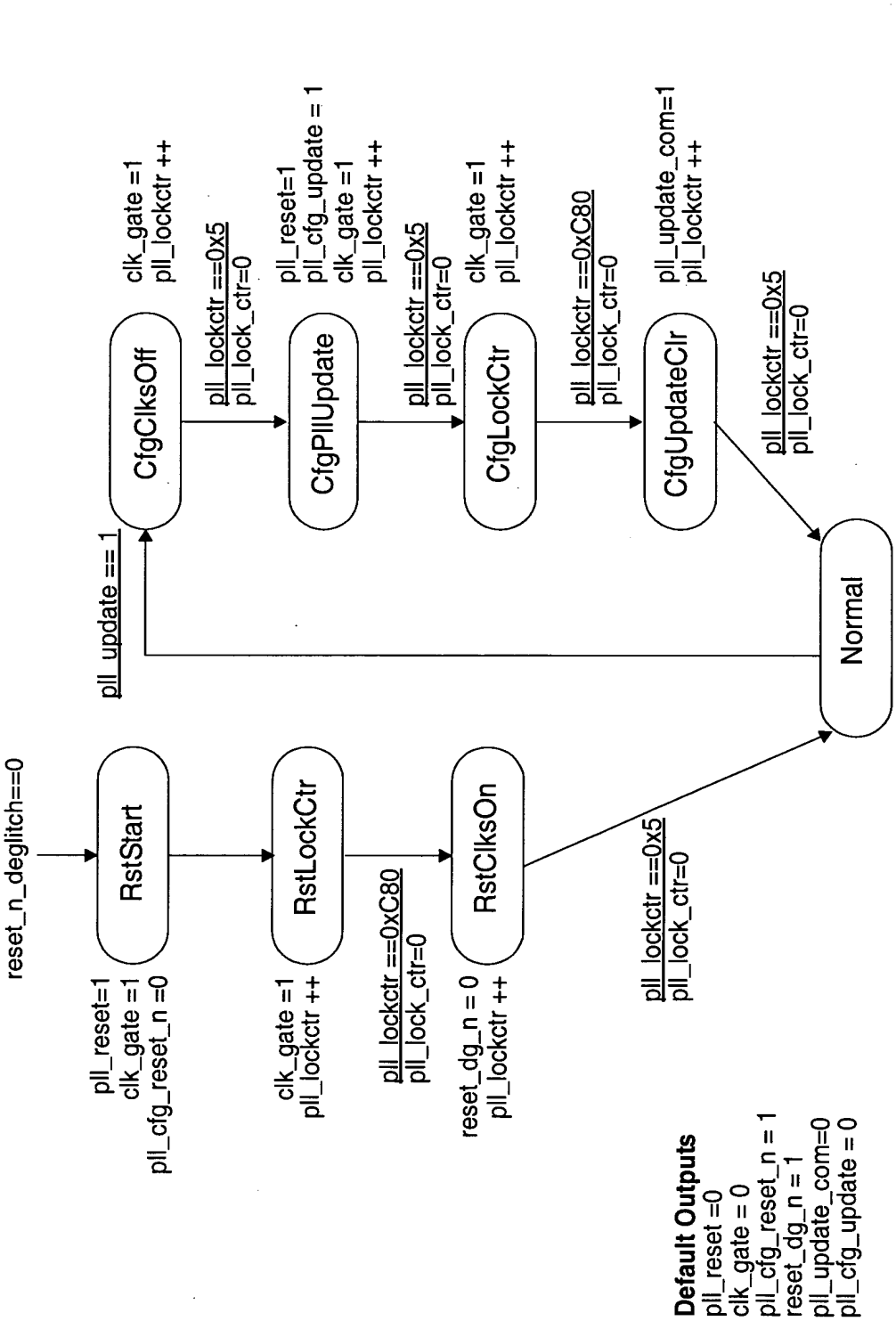
reset_n_deglitch==0
RstStart
pll_reset=1
clk_gate =1
pll_cfg_reset_n =0
RstLockCtr
clk_gate =1
pll_lockctr ++
pll_lockctr ==0xC80
pll_lock_ctr=0
RstClksOn
reset_dg_n = 0
pll_lockctr ++
pll_lockctr ==0x5
pll_lock_ctr=0
Normal
pll_update == 1
CfgClksOff
clk_gate =1
pll_lockctr ++
pll_lockctr ==0x5
pll_lock_ctr=0
CfgPllUpdate
pll_reset=1
pll_cfg_update = 1
clk_gate =1
pll_lockctr ++
pll_lockctr ==0x5
pll_lock_ctr=0
CfgLockCtr
clk_gate =1
pll_lockctr ++
pll_lockctr ==0xC80
pll_lock_ctr=0
CfgUpdateClr
pll_update_com=1
pll_lockctr ++
pll_lockctr ==0x5
pll_lock_ctr=0
Default Outputs
pll_reset =0
clk_gate = 0
pll_cfg_reset_n = 1
reset_dg_n = 1
pll_update_com=0
pll_cfg_update = 0

FIG. 20

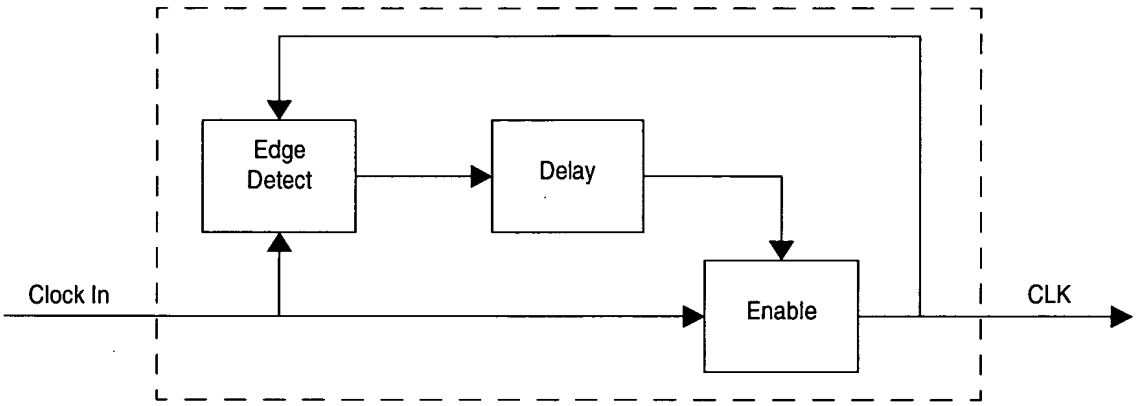

FIG. 21
(Prior Art)

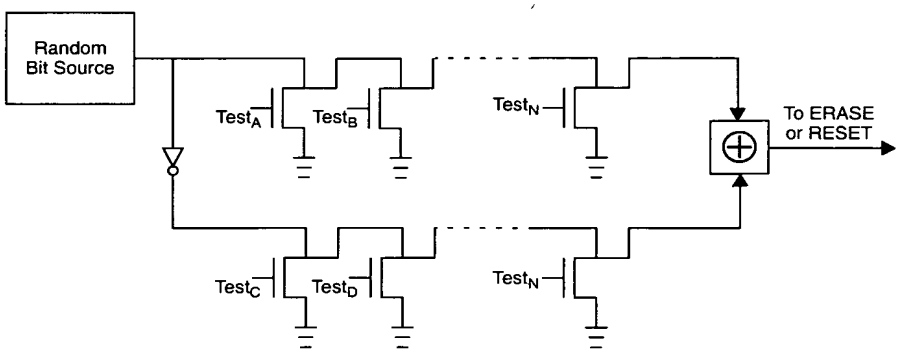
Random
Bit Source
Test$_A$
Test$_B$
Test$_N$
To ERASE
or RESET
Test$_C$
Test$_D$
Test$_N$

FIG. 22

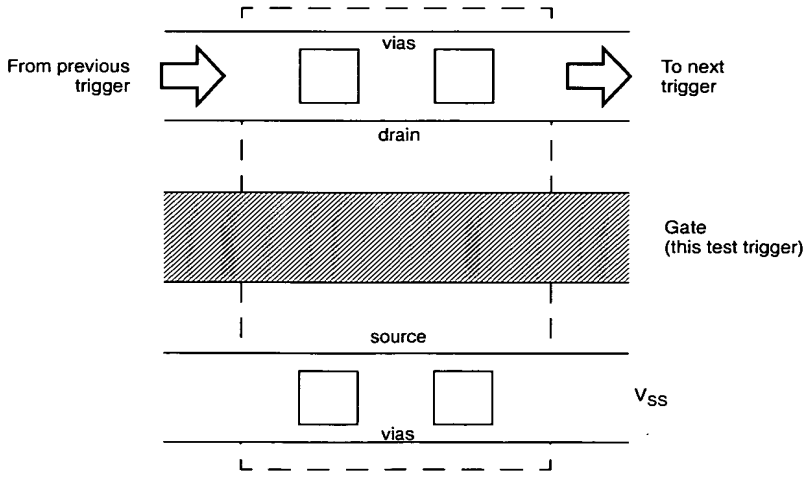
From previous
trigger
vias
To next
trigger
drain
Gate
(this test trigger)
source
V_{SS}
vias

FIG. 23

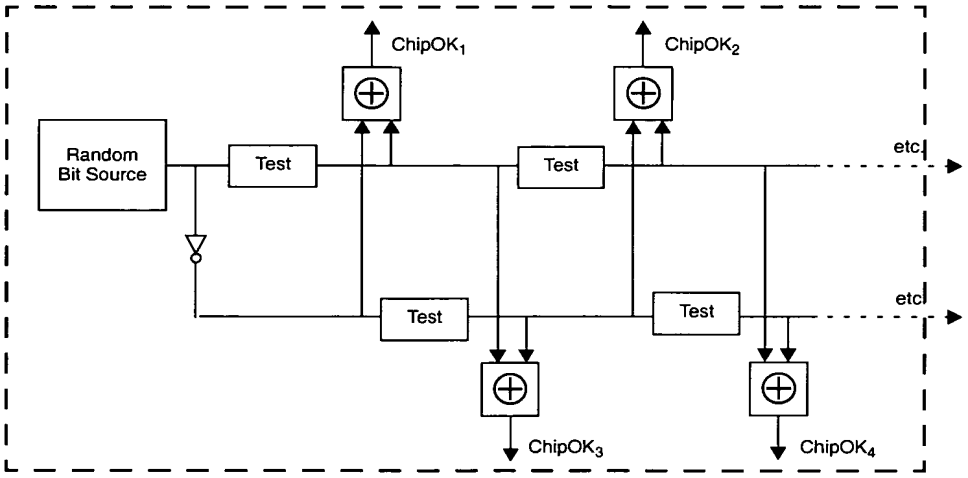
ChipOK1
ChipOK2
Random Bit Source
Test
Test
etc
Test
Test
etc
ChipOK3
ChipOK4

FIG. 24

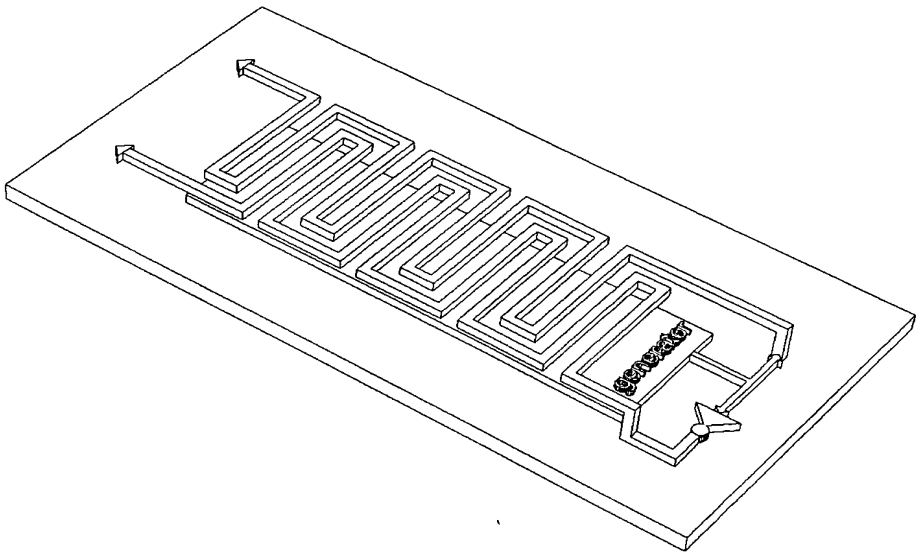

FIG. 25

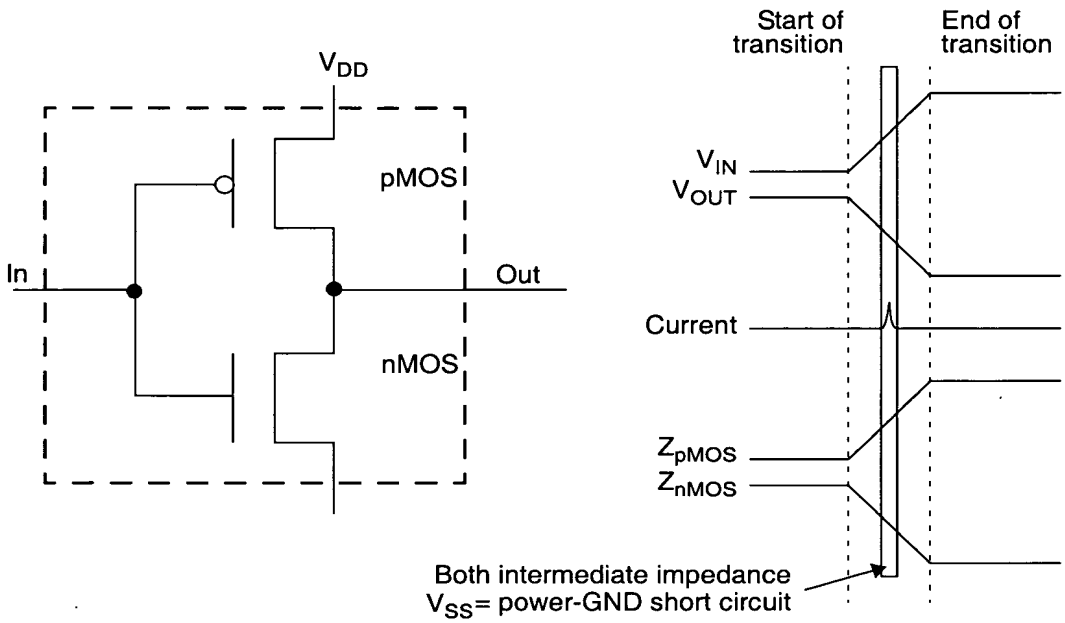

FIG. 26
(Prior Art)

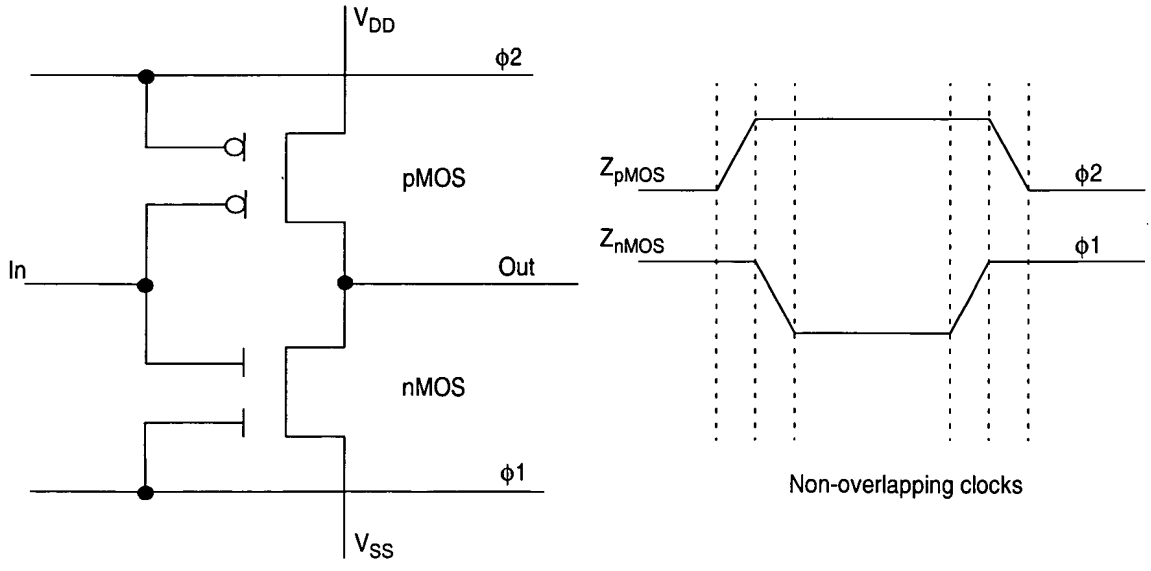

FIG. 27

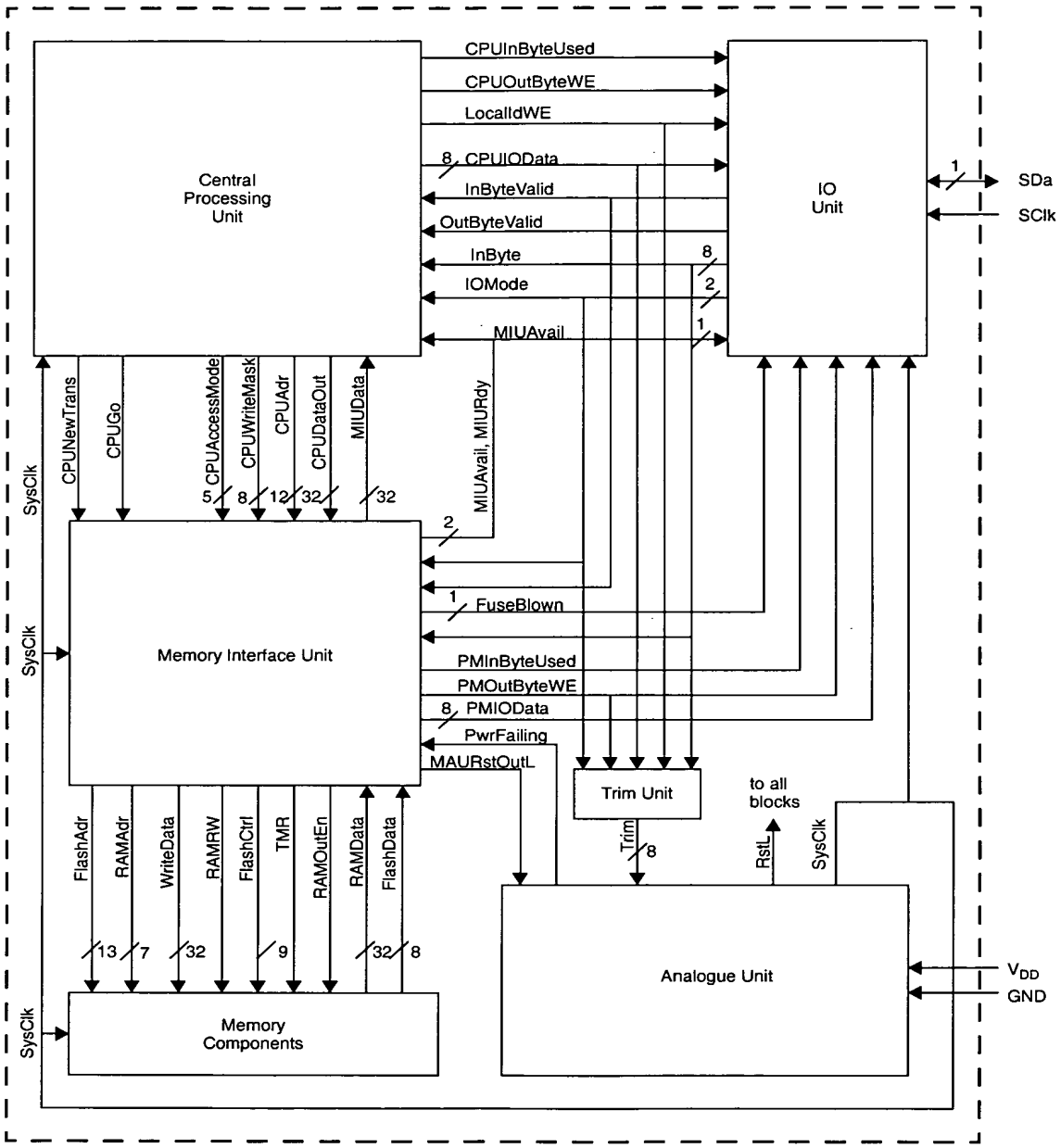
Central Processing Unit
IO Unit
Memory Interface Unit
Memory Components
Analogue Unit
Trim Unit
CPUInByteUsed
CPUOutByteWE
LocalIdWE
8 CPUIOData
InByteValid
OutByteValid
InByte
IOMode
MIUAvail
1 SDa
SClk
8
2
1
CPUNewTrans
CPUGo
CPUAccessMode
CPUWriteMask
CPUAdr
CPUDataOut
MIUData
MIUAvail, MIURdy
5 8 12 32 32
2
1 FuseBlown
PMInByteUsed
PMOutByteWE
8 PMIOData
PwrFailing
MAURstOutL
SysClk
FlashAdr
RAMAdr
WriteData
RAMRW
FlashCtrl
TMR
RAMOutEn
RAMData
FlashData
13 7 32 9 32 8
Trim
8
to all blocks
RstL
SysClk
VDD
GND

FIG. 28

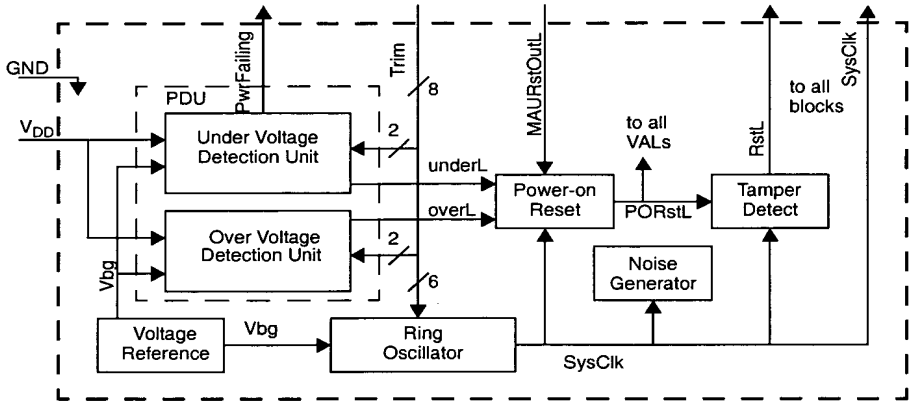

FIG. 29

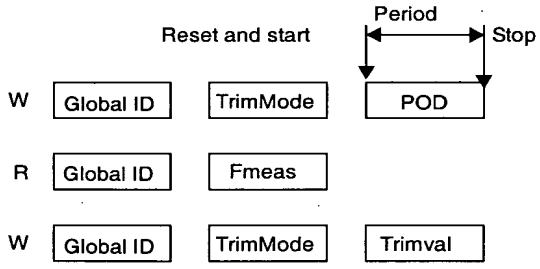

FIG. 30

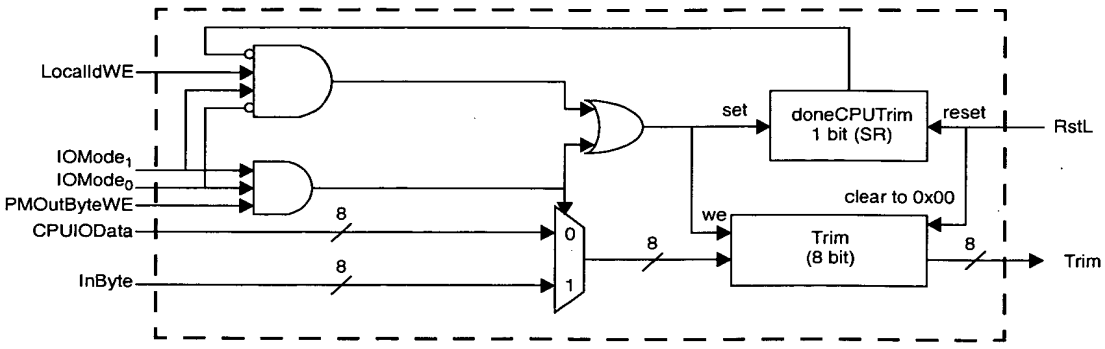

FIG. 31

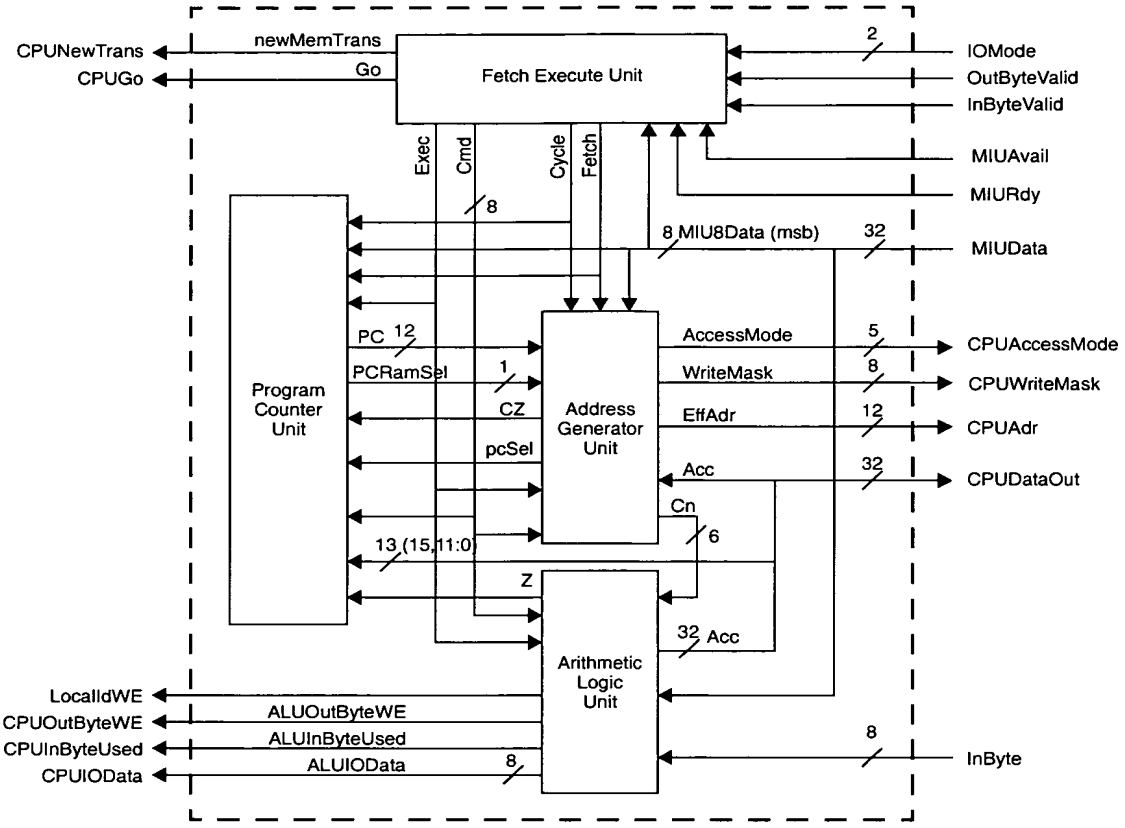
CPUNewTrans
CPUGo
newMemTrans
Go
Fetch Execute Unit
2
IOMode
OutByteValid
InByteValid
MIUAvail
MIURdy
Exec
Cmd
Cycle
Fetch
8
8 MIU8Data (msb)
32
MIUData
Program Counter Unit
PC 12
PCRamSel
1
CZ
pcSel
13 (15,11:0)
Address Generator Unit
AccessMode
5
CPUAccessMode
WriteMask
8
CPUWriteMask
EffAdr
12
CPUAdr
Acc
32
CPUDataOut
Cn
6
Z
32 Acc
Arithmetic Logic Unit
LocalIdWE
CPUOutByteWE
CPUInByteUsed
CPUIOData
ALUOutByteWE
ALUInByteUsed
ALUIOData
8
8
InByte

FIG. 32

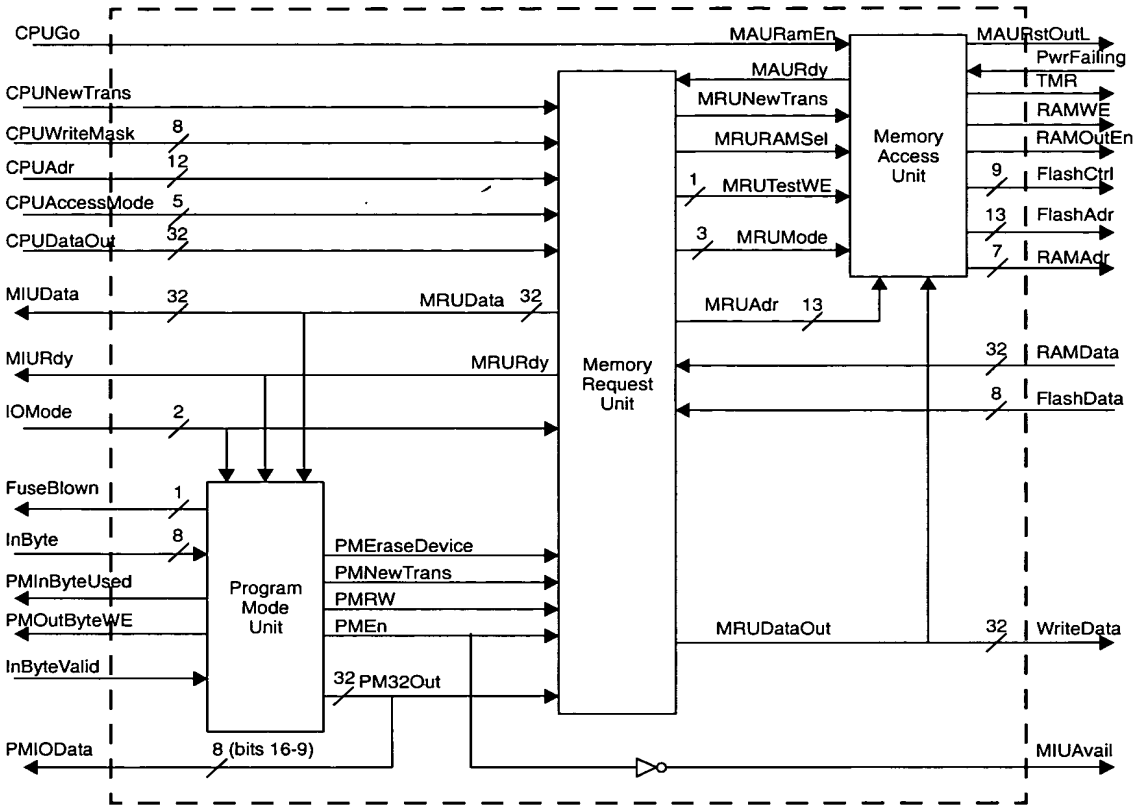
CPUGo
CPUNewTrans
CPUWriteMask
8
CPUAdr
12
CPUAccessMode
5
CPUDataOut
32
MIUData
32
MRUData
32
MIURdy
MRURdy
IOMode
2
FuseBlown
1
InByte
8
PMInByteUsed
PMOutByteWE
InByteValid
Program Mode Unit
PMEraseDevice
PMNewTrans
PMRW
PMEn
32 PM32Out
PMIOData
8 (bits 16-9)
Memory Request Unit
MAURamEn
MAURdy
MRUNewTrans
MRURAMSel
1
MRUTestWE
3
MRUMode
MRUAdr
13
MRUDataOut
Memory Access Unit
MAURstOutL
PwrFailing
TMR
RAMWE
RAMOutEn
9
FlashCtrl
13
FlashAdr
7
RAMAdr
32
RAMData
8
FlashData
32
WriteData
MIUAvail

FIG. 33

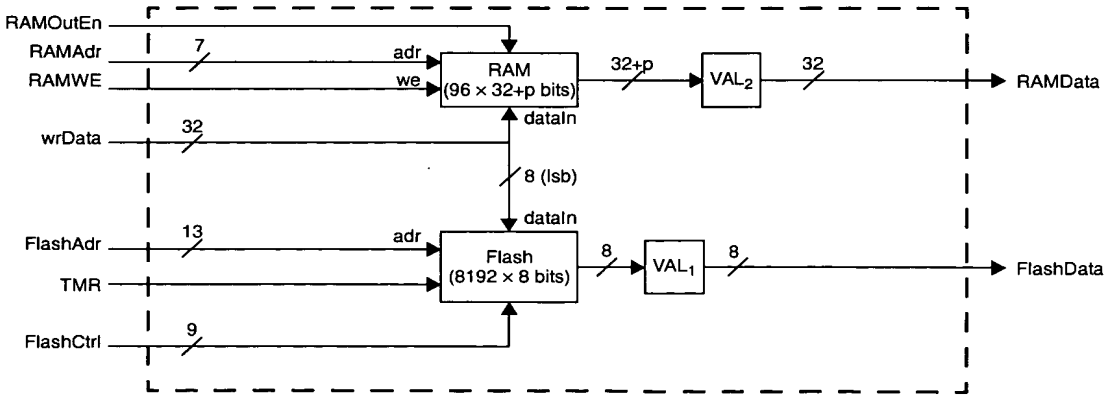
RAMOutEn
RAMAdr
7
RAMWE
adr
we
RAM
(96 × 32+p bits)
32+p
VAL2
32
RAMData
wrData
32
dataIn
8 (lsb)
dataIn
FlashAdr
13
TMR
FlashCtrl
9
adr
Flash
(8192 × 8 bits)
8
VAL1
8
FlashData

FIG. 34

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PrilD6	PrilD5	PrilD4	PrilD3	PrilD2	PrilD1	PrilD0	R/*W 0 = write 1 = read

FIG. 35

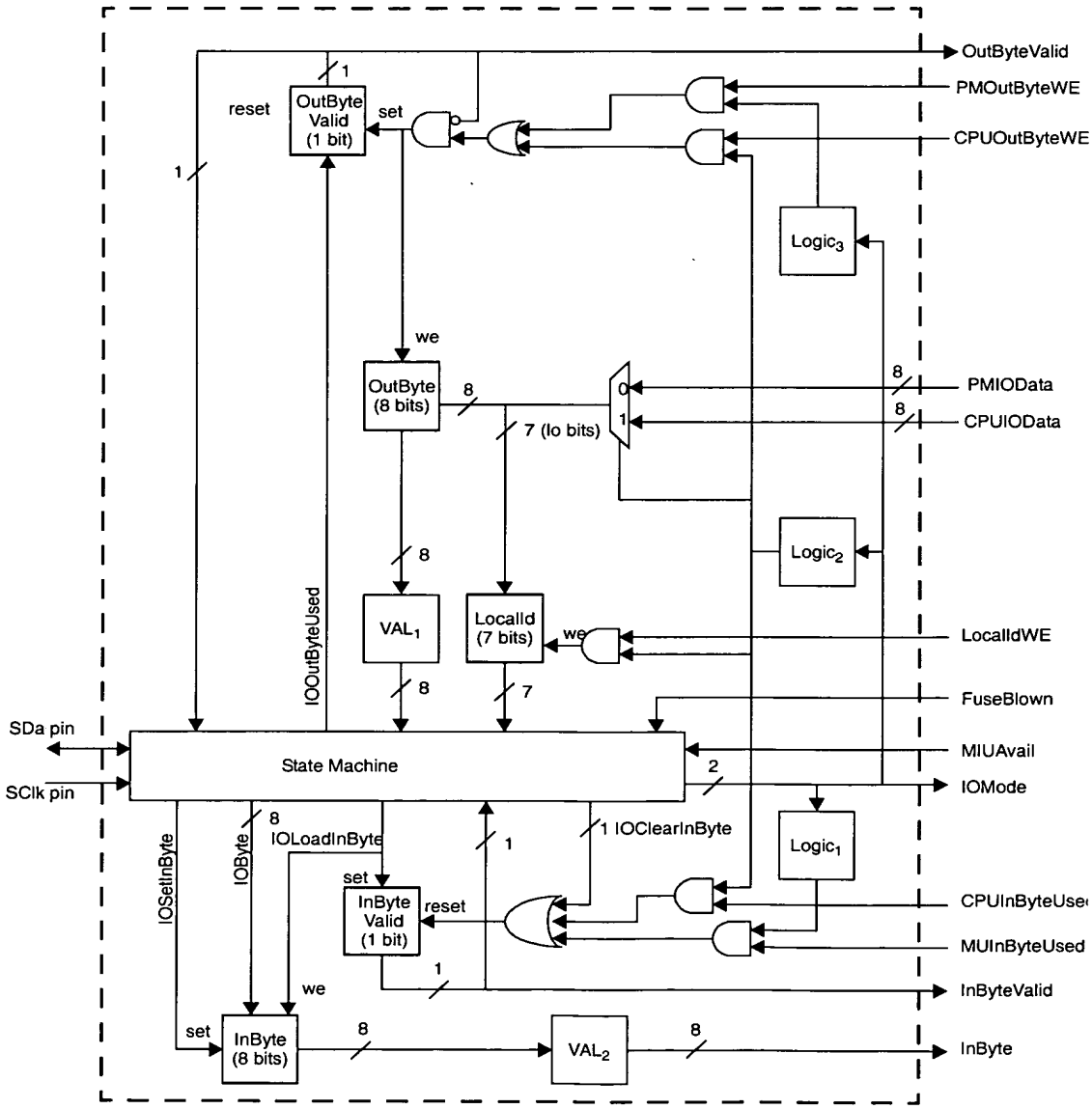

FIG. 36

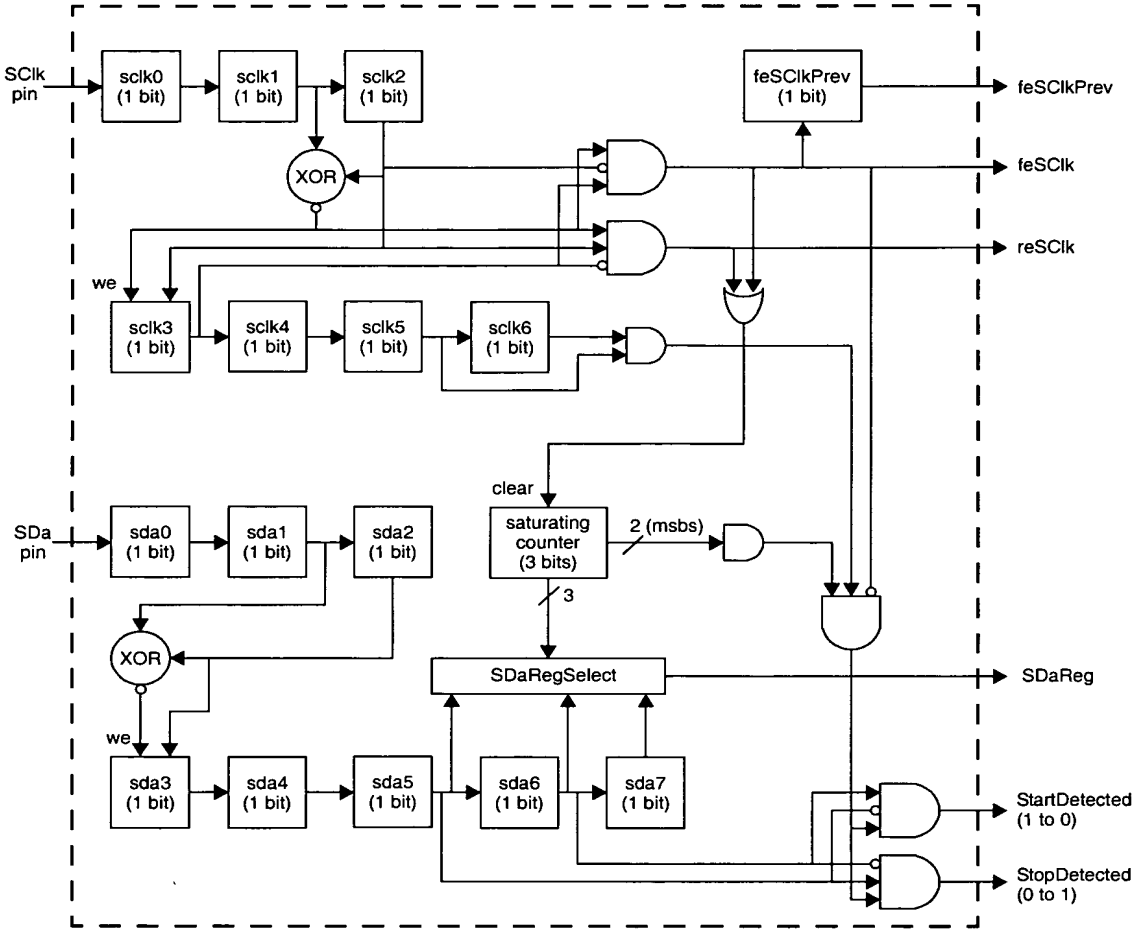
SClk pin
sclk0 (1 bit)
sclk1 (1 bit)
sclk2 (1 bit)
feSClkPrev (1 bit)
feSClkPrev
XOR
feSClk
reSClk
we
sclk3 (1 bit)
sclk4 (1 bit)
sclk5 (1 bit)
sclk6 (1 bit)
clear
SDa pin
sda0 (1 bit)
sda1 (1 bit)
sda2 (1 bit)
saturating counter (3 bits)
2 (msbs)
3
XOR
SDaRegSelect
SDaReg
we
sda3 (1 bit)
sda4 (1 bit)
sda5 (1 bit)
sda6 (1 bit)
sda7 (1 bit)
StartDetected (1 to 0)
StopDetected (0 to 1)

FIG. 37

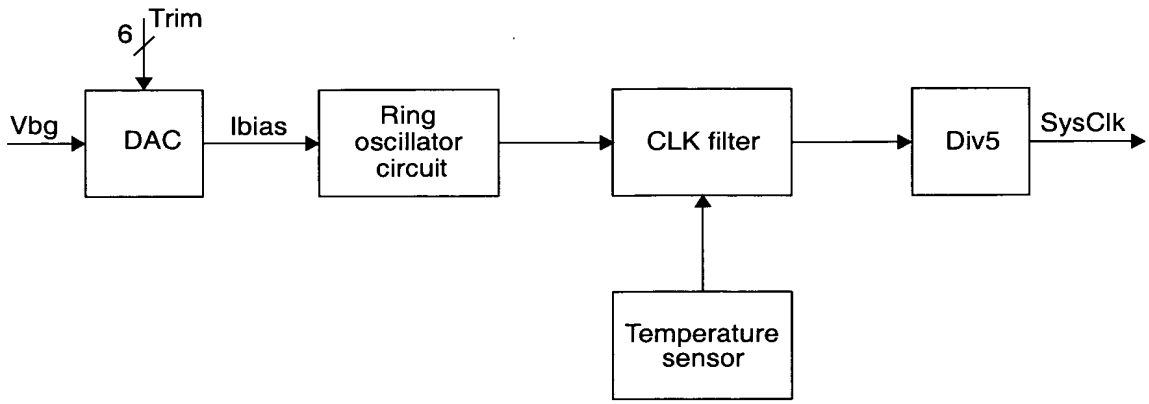
6
Trim
Vbg
DAC
Ibias
Ring oscillator circuit
CLK filter
Div5
SysClk
Temperature sensor

FIG. 38

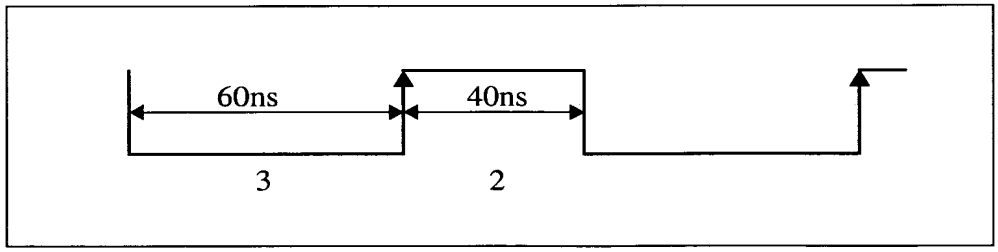
60ns
40ns
3
2

FIG. 39